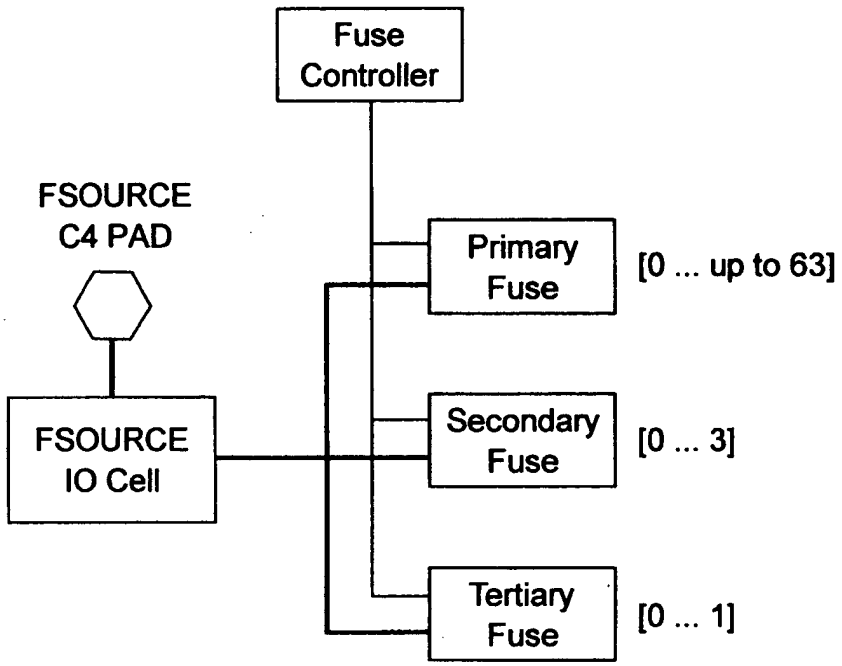
Annotated Marked-up Drawings

FIG. 1



Annotated Marked-up Drawings

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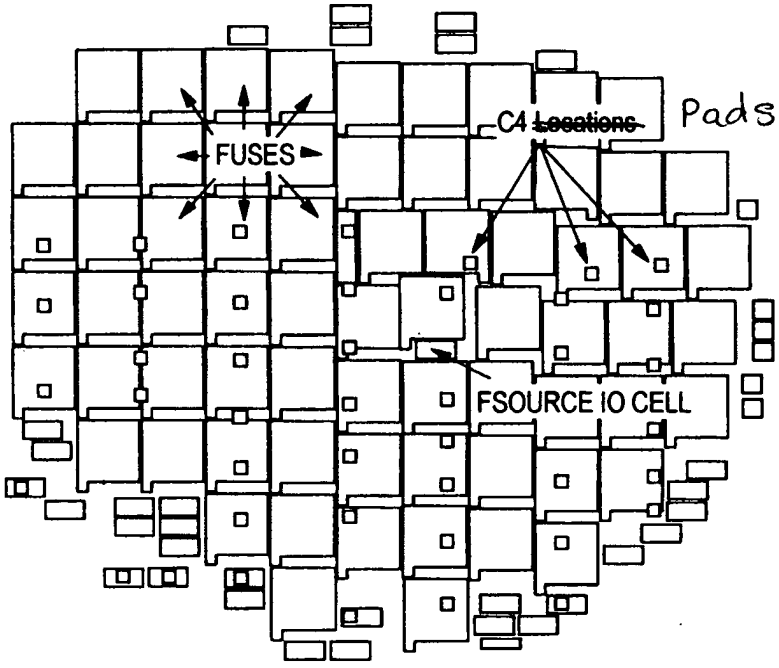
FIG. 2



Annotated Marked-up Drawings

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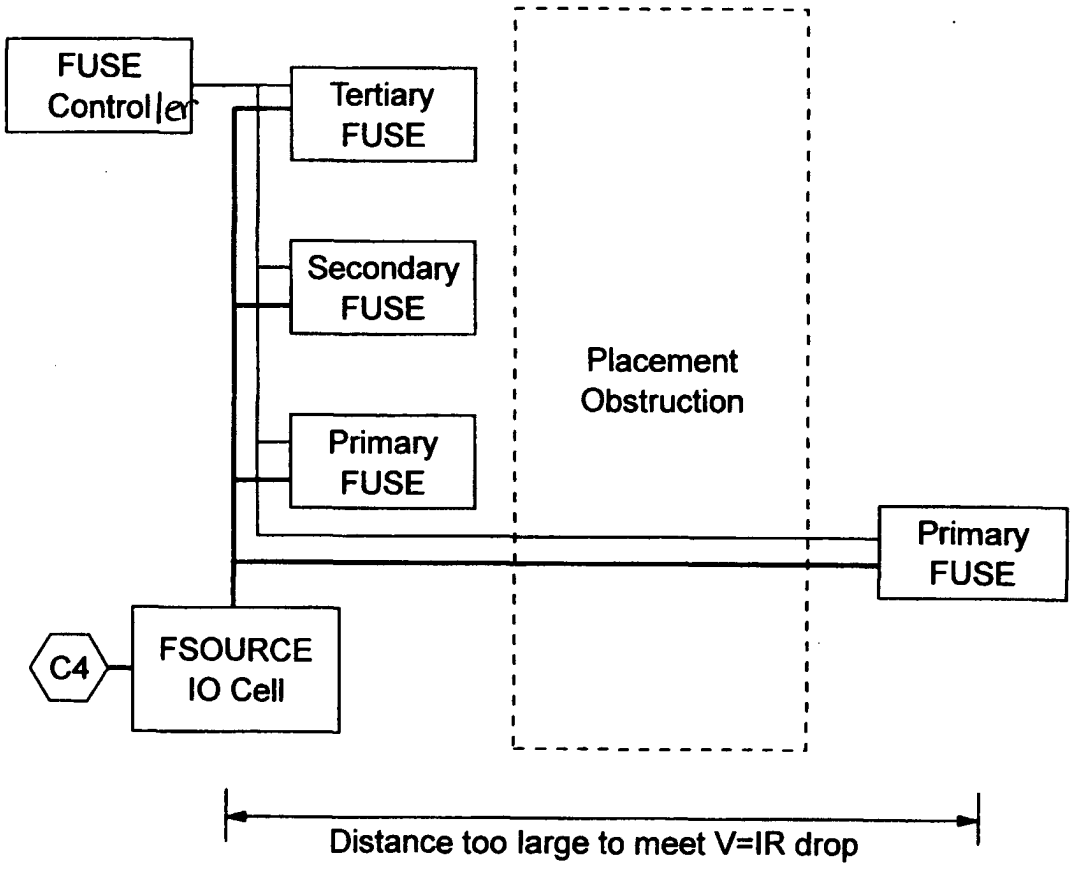
FIG. 3



Annotated Marked-up Drawings

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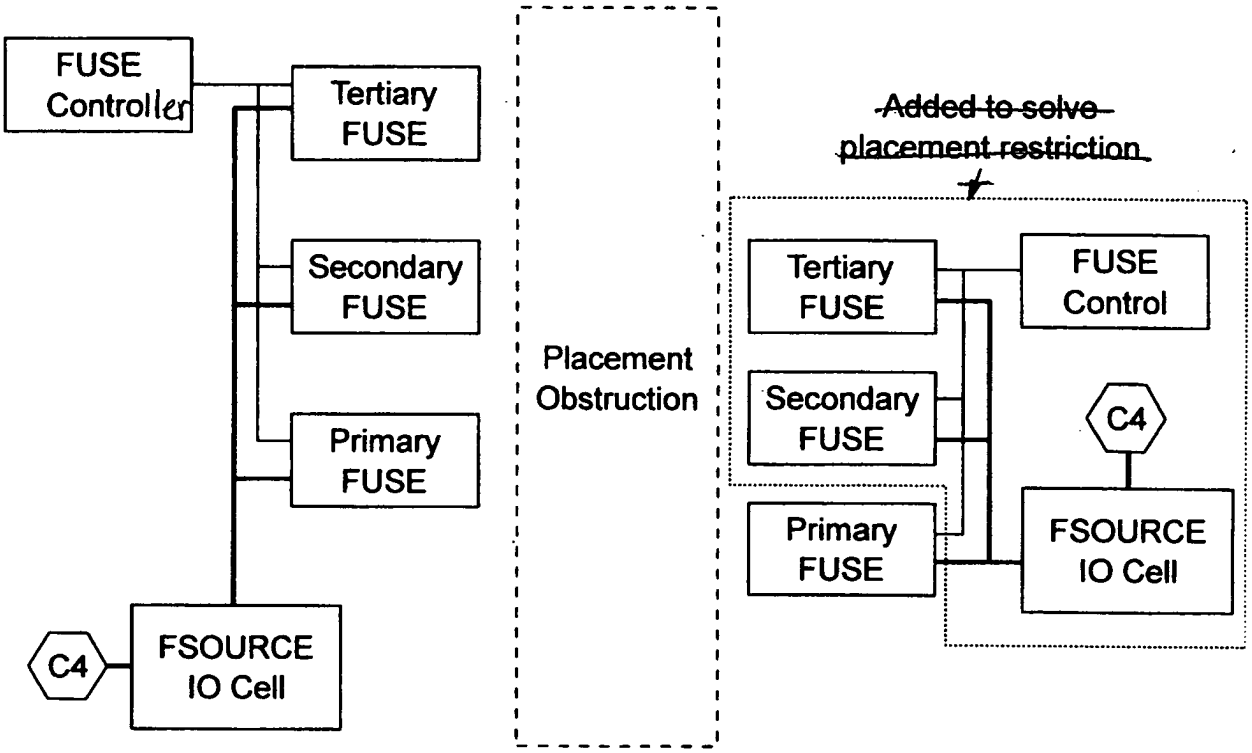
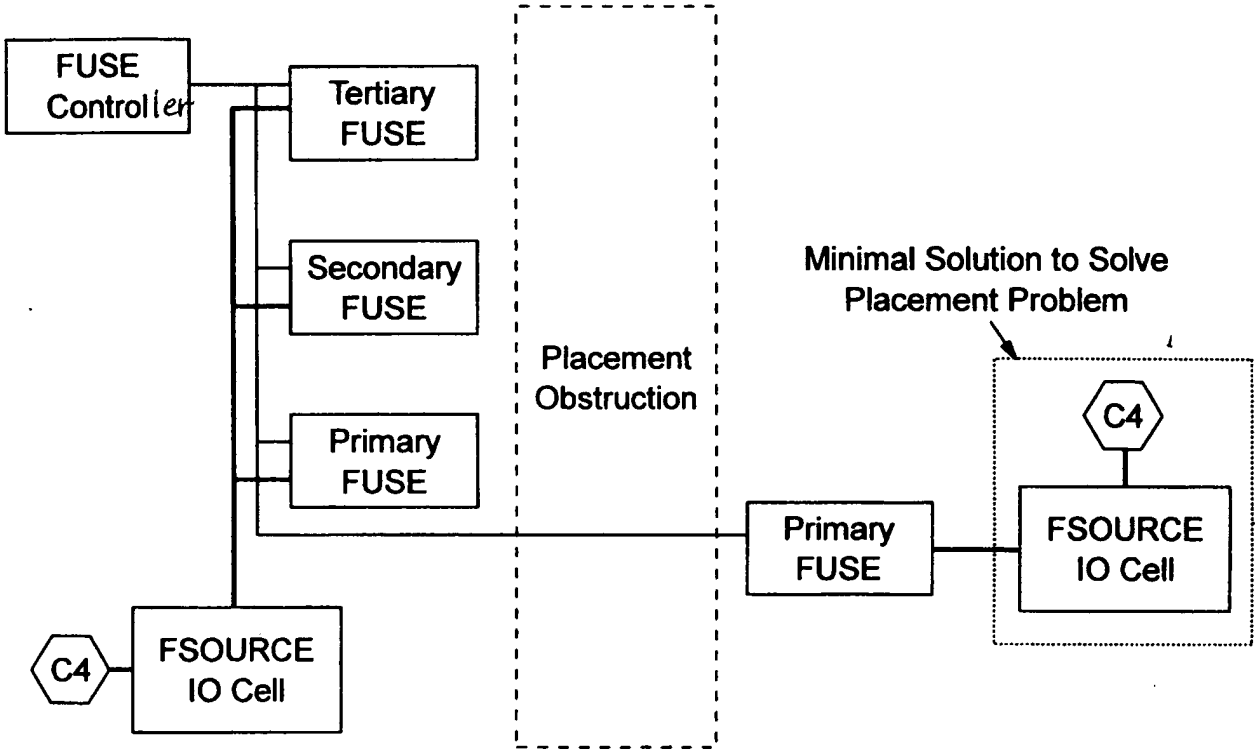
FIG. 4



Annotated Marked-up Drawings

FIG. 5



Annotated Marked-up Drawings

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FIG. 6

1. Determine P and N.

P = number of primary fuse macros
N = maximum allowable number of primary fuse macros per FSOURCE connection

2. Compare P and N and create FSOURCE C4s.

If P<N, create one FSOURCE C4
If P>N, create P/N (rounded up to nearest whole number) FSOURCE C4s

3. Divide primary fuse macros among FSOURCE C4s.

4. Floorplan the chip.

If normal floorplanning constraints cannot be met, go on to step 5.

5. ~~Create on new FSOURCE C4.~~ Increase number of FSOURCE C4s by one.

6. Divide primary fuse macros among FSOURCE C4s.

7. Repeat steps 4-6 until normal floorplanning constraints are met in Step 5.